AND8356

Performance of a 300 W, Wide Mains Interleaved PFC Driven by the NCP1601

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APPLICATION NOTE

Overview

AND8354 gives the key steps to designing an interleaved PFC driven by two NCP1601. The goal of this paper is to present a board that has been developed following this process. Its specification is the following one:

- *Maximum output power: 300 W*
- *Input voltage range: from 90 V_{rms} to 265 V_{rms}*
- *Regulation output voltage: 390 V*
- *Clamp frequency: 120 kHz*

In this application note, a special attention is paid to the efficiency at full and light load and to other merits of interleaving as detailed in AND8355.

Introduction

Interleaving consists in paralleling two “small” stages in lieu of a bigger one, which may be more difficult to design. Practically, two 150 W PFC stages are combined to form our 300 W PFC pre−regulator. As detailed in AND8355, this approach has several merits like the ease of implementation, the use of more but smaller components or a better heat distribution.

Also, interleaving extends the power range of Critical Conduction Mode (CrM) that is an efficient and cost−effective technique (no need for low t_{rr} diodes). Superior efficiency levels are even achievable when associated to the Frequency Clamped Critical conduction Mode (FCCrM) that is a unique scheme developed by ON Semiconductor to reduce the switching losses without sacrificing the PF and THD performance.

Furthermore, if the two stages are operated out−of−phase, the current ripple is significantly reduced. In particular, the input current exhibits a moderate ripple like that of a PFC stage operating in continuous conduction mode (CCM). Also, the rms current within the bulk capacitor is dramatically reduced.

This paper reports the main performance of a discrete solution for interleaved PFC. As detailed in AND8354, two NCP1601 circuits are implemented to control the operation of the PFC stage (one controller per branch). The two branches are operating independently but some circuitry is applied to the synchronization pins of the two devices to obtain a substantial out−of−phase operation.

The NCP1601 is an 8−pin device that drives each phase in Frequency Clamped Critical conduction Mode (FCCrM). As a voltage mode controller, it forces the MOSFET on−time that is identical for both branches as long as the two circuits share the same control voltage (practically the pin2 that makes available the output of the regulation blocks of each of the two circuits are connected together).

A comprehensible overview of the interleaving characteristics and details regarding the application design steps are given in AND8355 and AND8354 respectively. Please refer to them for further information.

BOARD PHOTOGRAPH

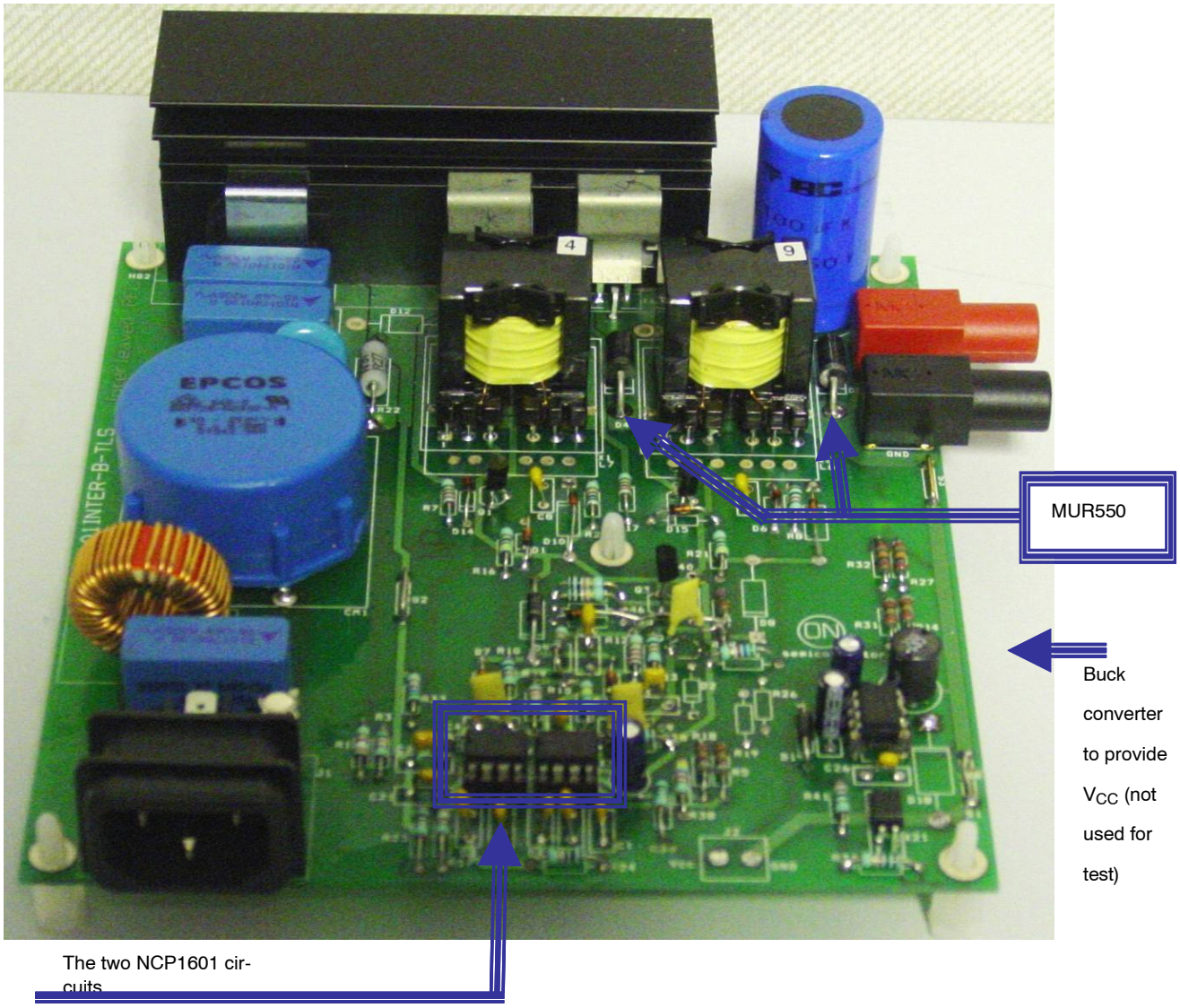

Figure 1. Application Schematic

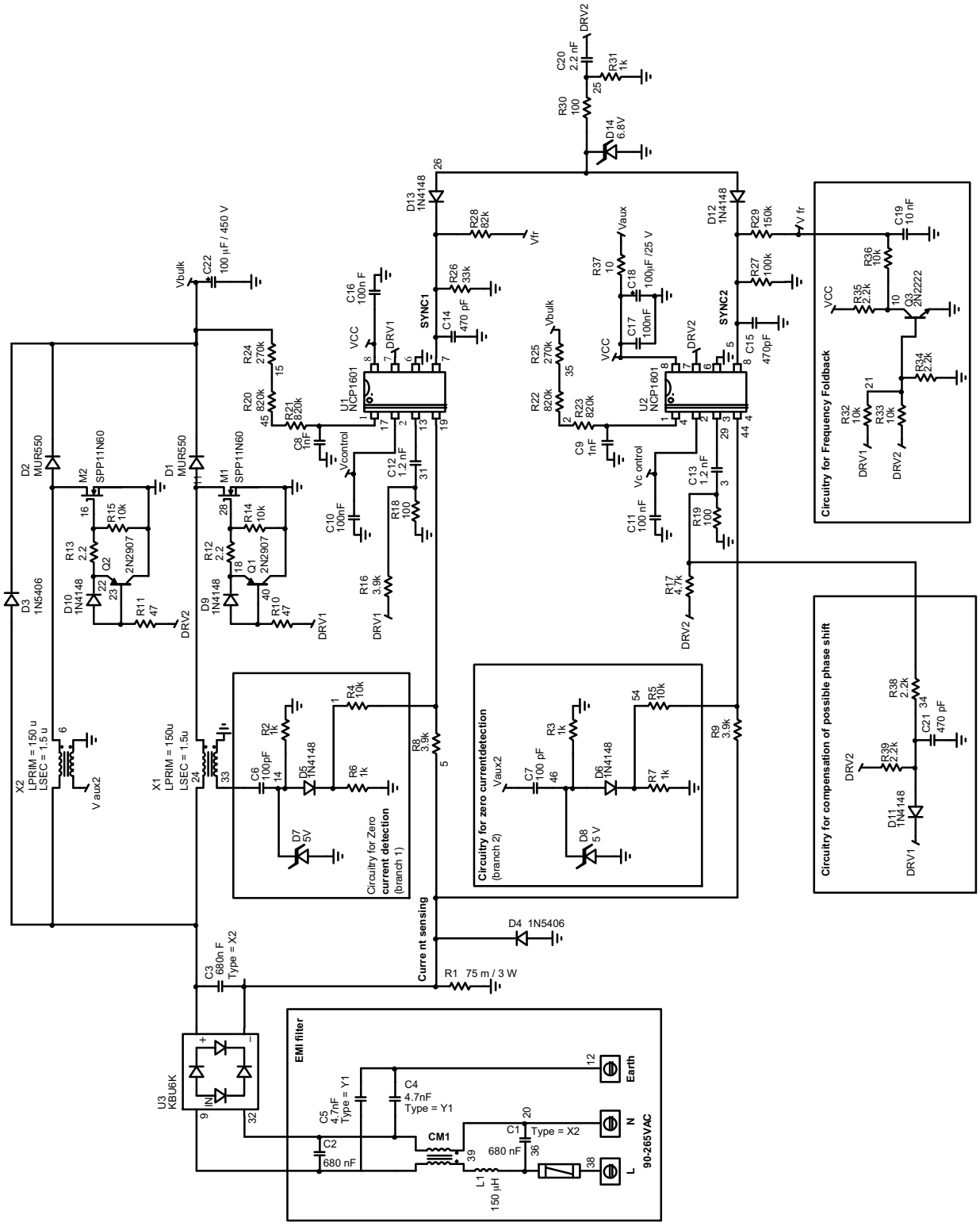

Figure 2. Application Schematic

BILL OF MATERIAL

Designator	Quantity	Description	Value	Manufacturer	Part number
C1, C2, C3	3	275 V, X2 capacitor	680 nF	RIFA	PHE840MF6680M
C4, C5	2	275 V, Y capacitor	4.7 nF	muRata	DE1E3KX472MA5B
C6, C7	2	ceramic capacitor	100 pF / 50 V	various	
C8, C9	2	ceramic capacitor	1 nF / 50 V	various	
C10, C11, C16, C17	4	ceramic capacitor	100 nF / 50V	various	
C12, C13	2	ceramic capacitor	1.2 nF / 50 V	various	
C14, C15, C21	3	ceramic capacitor	470 pF / 50 V	various	
C18	1	electrolytic capacitor	100 μF / 25 V	various	
C19	1	ceramic capacitor	10 nF / 50 V	various	
C20	1	ceramic capacitor	2.2 nF / 50 V	various	
C22	1	electrolytic capacitor	100 μF / 450 V	BC Components	222 215 937 101
R1	1	+/− 1%, 3 W resistor	75 m	Vishay	RLP3 0R075 1%
R2, R3, R6, R7, R31	5	¼ W resistor	1 kΩ	various	
R4, R5, R14, R15, R32, R33, R36	7	¼ W resistor	10 kΩ	various	
R8, R9, R16	3	¼ W resistor	3.9 kΩ	various	
R10, R11	2	¼ W resistor	47 Ω	various	
R12, R13	2	¼ W resistor	2.2 Ω	various	
R17	1	¼ W resistor	4.7 kΩ	various	
R18, R19, R30	3	¼ W resistor	100Ω	various	
R20, R21, R22, R23	4	¼ W resistor	820 kΩ	various	
R24, R25	2	¼ W resistor	270 kΩ	various	
R26	1	¼ W resistor	33 kΩ	various	
R27	1	¼ W resistor	100 kΩ	various	
R28	1	¼ W resistor	82 kΩ	various	
R29	3	¼ W resistor	150 kΩ	various	
R34, R35, R38, R39	4	¼ W resistor	2.2 kΩ	various	
R37	1	¼ W resistor	10 Ω	various	
Q1, Q2	2	TO92, PNP transistor	2N2907	ON Semiconductor	P2N2907AG
Q3	1	TO92, NPN transistor	2N2222	ON Semiconductor	P2N2222AG
D1, D2	2	Axial, 520 V, Ultrafast diode	MUR550	ON Semiconductor	MUR550APFG
D3, D4	4	600 V, standard recovery diode	1N5406	ON Semiconductor	1N5406G
D5, D6,D9, D10, D11, D12, D13	7	diode	1N4148	Philips	1N4148
D7, D8	2	5 V Zener diode		various	
D14	1	6.8 V Zener diode		various	
L1	1	DM Choke	150μH/5A, WI−FI series	Wurth Elektronik	
CM1	1	CM1 Filter (4A, 2*6.8mH).	B82725−J2402−N20	EPCOS	
X1, X2	2	PFC coil	86H−7416	Delta	86H−7416
M1, M2	2	MOSFET	SPP11N60S5	Infineon	SPP11N60S5
U3	1	Diodes Bridge	KBU6K	General Semiconductor	
U1, U2	2	DIP8 controller	NCP1601B	ON Semiconductor	NCP1601BPG
Heatsink	1	Heatsink (2.9°C/W)	437479	AAVID THERMALLOY	
Fuse	1	4 A fuse		various	

GENERAL BEHAVIOR

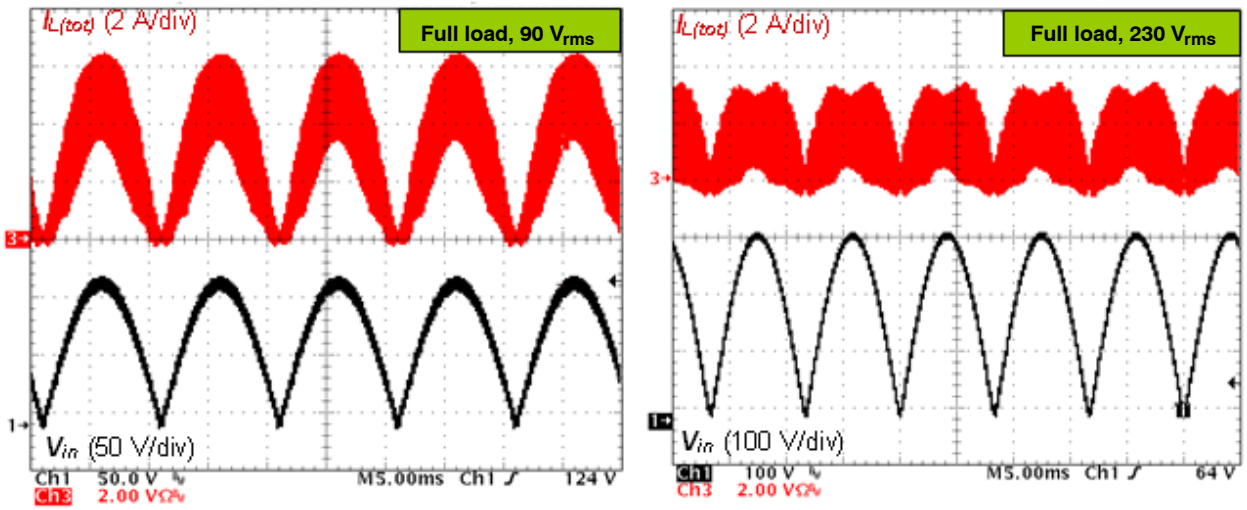

Figure 3. Input Current and Voltage at Low and High Line

Plots of Figure 3 portray the input voltage and current of the interleaved PFC stage. More specifically, $I_{L(tot)}$ is the total current drawn by the two branches. The measurements were done at low and high line (90 V_{rms} – left plot – and 230 V_{rms} – right plot).

As explained in AND8355, interleaving with a 180° phase shift minimizes the input current ripple. Finally, two CrM or FCCrM PFC stages operated out−of−phase absorbs an input current that looks like that obtained with a Continuous Current Mode (CCM) PFC stage.

At low line, the current waveform exactly matches the theoretical one that is derived in AND8355. At high line, the waveform remains relatively similar to the computed shape but does not match completely because of the frequency fold−back that tends to slightly increase the ripple. This is not an issue since the current is low at high line.

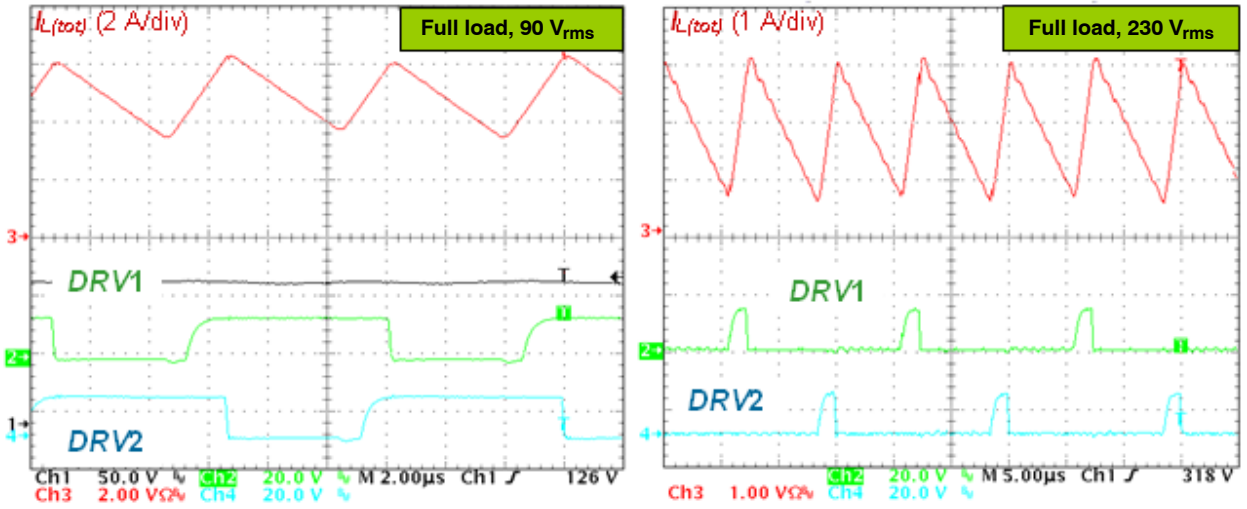

Figure 4. Zoom at the Sinusoid Top

Plots of Figure 4 were obtained at the sinusoid top. In this figure, the drivers are shown to highlight the out−of−phase operation (***DRV1*** and ***DRV2*** are the drive signals for branch 1 and branch 2, respectively).

These figures attest that at low and high line, the phase shift is substantially 180°. They also confirm that the total input current swings at twice the frequency of each phase.

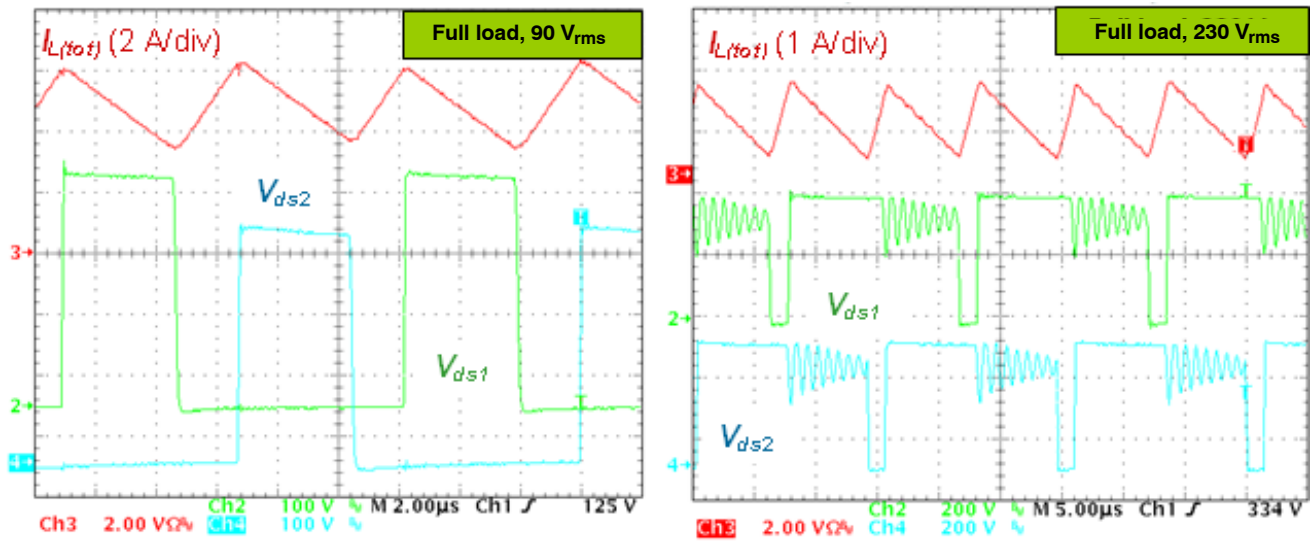

Figure 5. Another Zoom at the Sinusoid Top

Figure 5 still portrays the input current at low and high line but compared to the precedent one, the MOSFET drain−source voltage replaces the drive signal for the two branches.

These plots show that:

- At low line, each phase operates in critical conduction mode with valley switching for an optimized efficiency. There is no overlap between the demagnetization sequences of each phase. The diode current of branch 1 does not add to the diode current of branch 2. On the contrary, these currents are interleaved for a minimized ac content of the bulk capacitor current.
- At high line, the two branches operate in fixed frequency. The frequency fold−back function even leads to a relative low frequency operation (about 50 kHz). This helps to further improve the efficiency in a condition where the switching losses are the main ones. In CrM, the demagnetization phases would overlap since the core reset sequence is the preponderant phase.

PERFORMANCE

The board performance are measured in the following conditions:

- The measurements were made after the board was 30 mn operated at full load, low line
- All the measurements were made consecutively without interruption
- PF, THD, $I_{in(rms)}$ were measured by a power meter Voltech PM1200
- $V_{in(rms)}$ was measured directly at the input of the board by a HP 34401A multi−meter
- V_{out} was measured by a HP 34401A multi−meter
- The input power was computed according to:

$$P_{in(avg)} = V_{in(rms)} \cdot I_{in(rms)} \cdot PF$$

- Open frame, ambient temperature, no fan

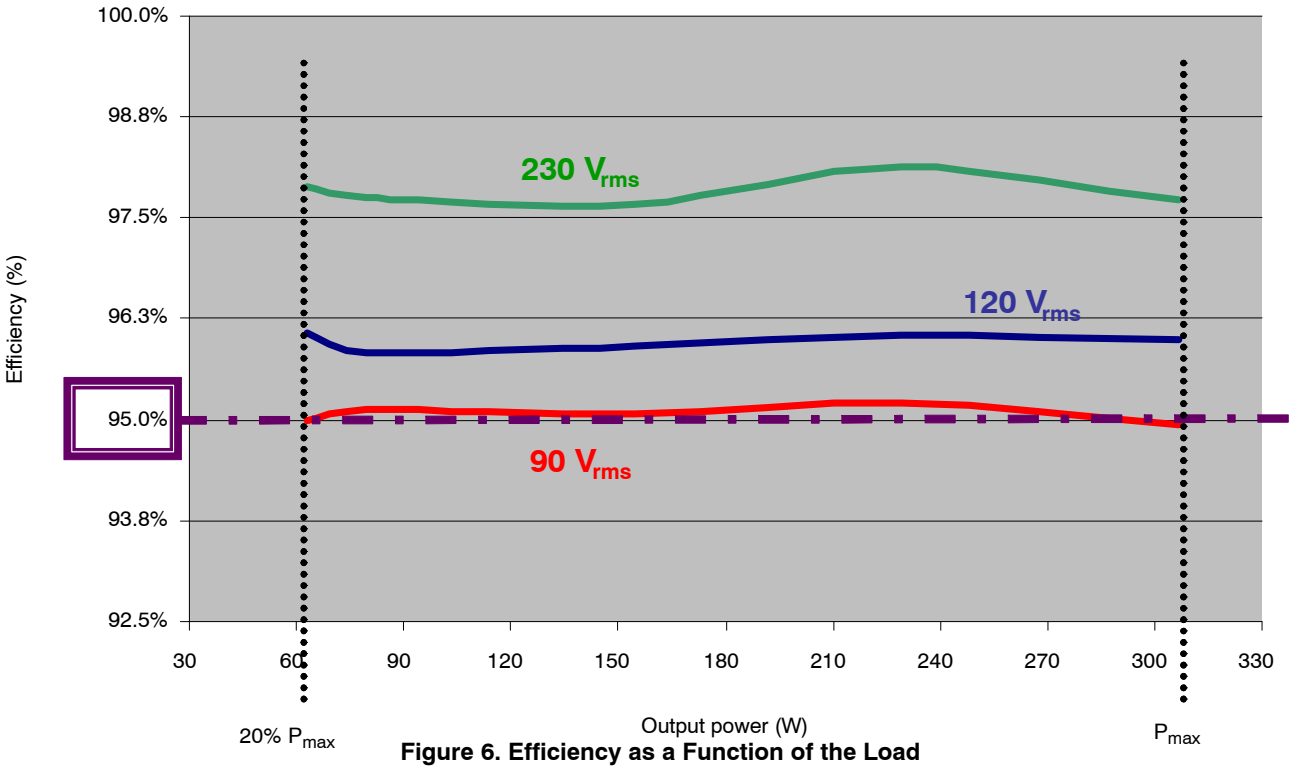

Figure 6. Efficiency as a Function of the Load

Figure 6 portrays the efficiency over the line range, from 20% to 100% of the load.

The efficiency remains higher than 95% at low line (90 V_{rms}).

It is worth noting that this flat curve is due to the FCCrM (frequency clamped CrM) operation that prevents the switching frequency from increasing at light load. Due to this, the efficiency remains high in light load while it would be dramatically degraded by the switching losses in CrM.

It should also be noted that these results are obtained in a relatively high frequency application. To limit the inductor size and cost, each branch features a 150 μH coil which leads to a 85 kHz switching frequency at full load, low line (top of the sinusoid). Figure 8 details the switching frequency range of the application. A lower frequency application could even exhibit a higher efficiency (minimized switching losses in the MOSFETs and inductors) at the cost of bigger coils.

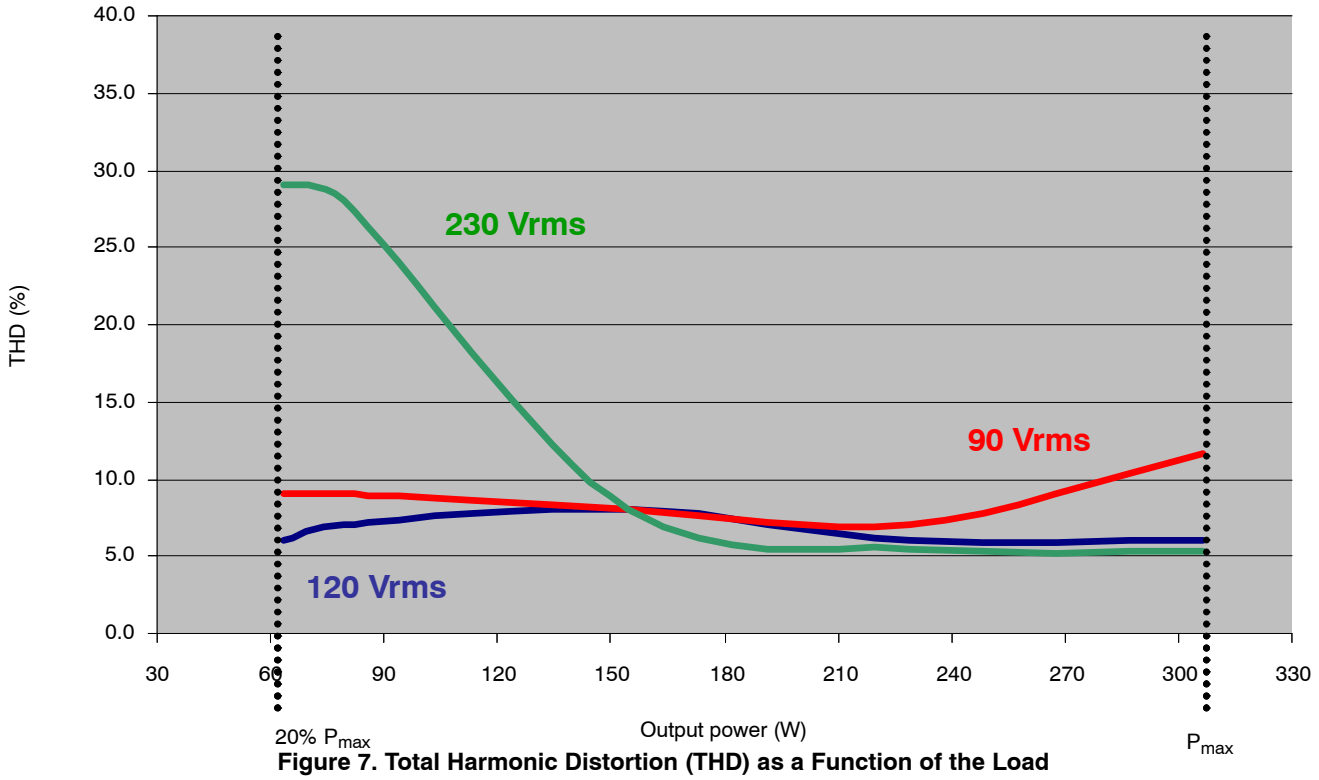

Figure 7. Total Harmonic Distortion (THD) as a Function of the Load

Figure 7 shows the total harmonic distortion (THD) over the line range, from 20% to 100% of the load. The THD is extremely low at low line and slightly increases at high line, light load without becoming excessive. **THD remains low on the whole range**

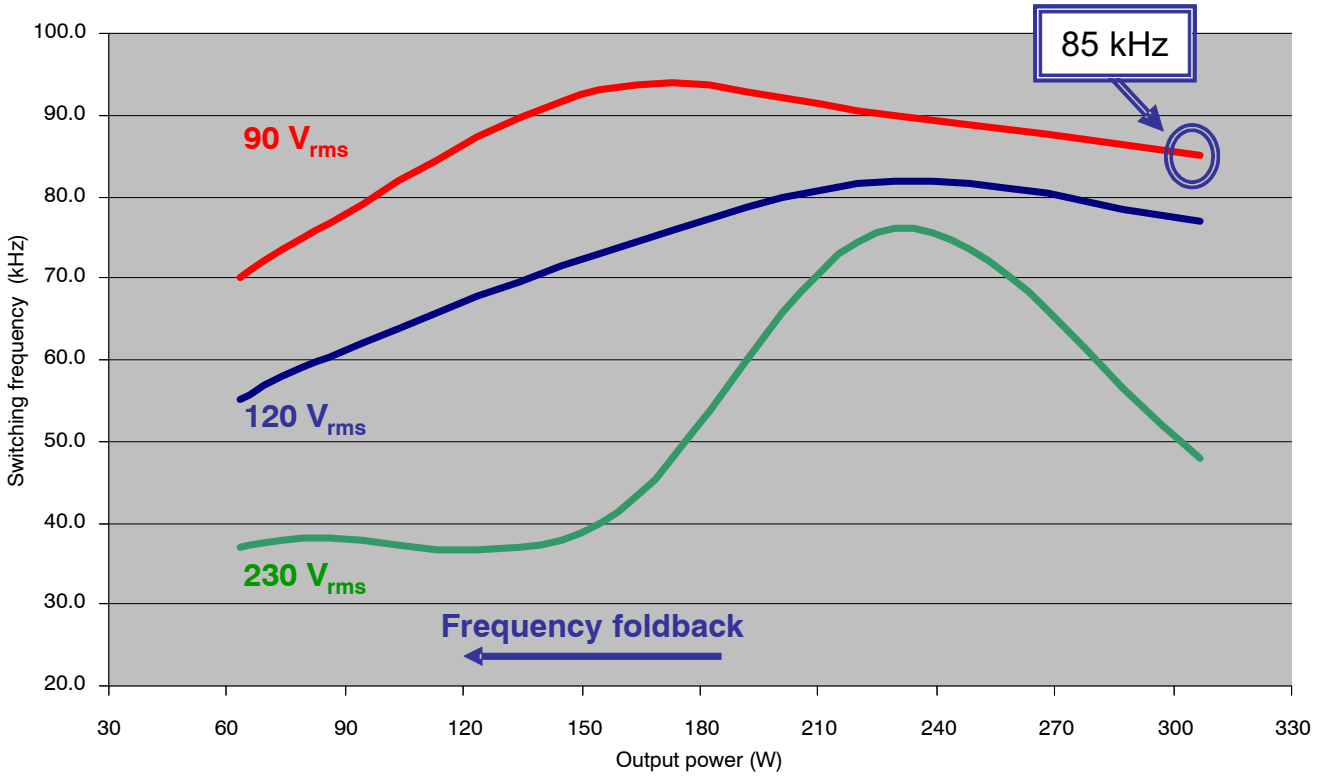

Figure 8. Switching Frequency versus Load (Top of the Sinusoid)

Figure 8 portrays the switching frequency variation (at the sinusoid top) as a function of the load and over the line range. The curves apply to each branch. The switching frequency of the interleaved PFC stage is twice. As aforementioned, the application operates at a relatively high frequency at low line to limit the inductor size and cost (85 kHz per branch at low line, full load). At light load and/or high line, frequency fold−back lowers the switching frequency. This function enables to maintain a high efficiency when the power is low as portrayed by Figure 6.

CONCLUSION

This application note reports the main experimental results obtained using a 300 W, interleaved PFC stage where each interleaved branch is driven by a NCP1601, that is, a PFC controller operating in Frequency Clamped Critical conduction Mode. AND8354 details the design steps to implement this solution.

This application confirms the analytic computations of AND8355. More specifically, we could check that out−of−phase interleaving:

- Reduces the input current ripple
- Lower the bulk capacitor rms current

The solution was designed to operate at relatively high frequency to limit the inductor size and cost (the selected 150 μH coils lead to a 85 kHz switching frequency per each branch at full load, low line − top of the sinusoid). Despite this, the application is particularly efficient. Efficiency is higher than 95% at 90 V_{rms} over a large load range (from 20% to 100% load).

Besides interleaving, this solution takes also benefit of:

- The use of MUR550 diodes optimized for discontinuous mode PFC applications.
- Frequency fold−back that optimizes the light load performance.
- The FCCrM mode that optimizes the efficiency in all conditions.

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